(19) Europäisches Patentamt
European Patent Office
Office Européen des brevets

(11) Publication number: 0 223 920 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification: 02.01.91 Bulletin 91/01

(51) Int. Cl.⁵: H01L 21/306, H01L 21/60

(21) Application number: 86110461.0

(22) Date of filing: 29.07.86

(54) Chem-mech polishing method for producing coplanar metal/insulator films on a substrate.

The file contains technical information submitted after the application was filed and not included in this specification

(30) Priority: 28.10.85 US 791860

(43) Date of publication of application: 03.06.87 Bulletin 87/23

(45) Publication of the grant of the patent: 02.01.91 Bulletin 91/01

(84) Designated Contracting States: DE FR GB IT

(56) References cited:
EP-A- 0 013 508
FR-A- 2 256 260
US-A- 3 836 473
IBM TECHNICAL DISCLOSURE BULLETIN, vol. 24, no. 4, September 1981, page 2138, New York, US; C.H. SCRIVNER, Jr.: "Polishing technique to remove aluminum lands from semiconductor chips"
JOURNAL OF THE ELECTROCHEMICAL SOCIETY, vol. 122, no. 7, July 1975, pages 931-936, New York, US; J.J. KELLY et al.: "An electrochemical study of undercutting during etching of duplex metal films"

(73) Proprietor: International Business Machines Corporation
Old Orchard Road
Armonk, N.Y. 10504 (US)

(72) Inventor: Beyer, Klaus Dietrich
3 Tamidan Road
Poughkeepsie New York 12601 (US)
Inventor: Guthrie, William Leslie
394 Van Wyck Lake Road
Hopewell Junction New York 12533 (US)
Inventor: Markarewicz, Stanley Richard
17 Cherry Avenue
New Windsor New York 12550 (US)
Inventor: Mendel, Eric
3 High Point Drive
Poughkeepsie New York 12603 (US)
Inventor: Patrick, William John
3 Rockwood Drive
Newburgh new York 12550 (US)
Inventor: Perry, Kathleen Alice
Rd 1, Box 17 Upton Road
Lagrangeville New York 12540 (US)
Inventor: Pliskin, William Aaron
31 Greenvale Farms Road
Poughkeepsie New York 12603 (US)
Inventor: Riseman, Jacob
38 Barnard Avenue
Poughkeepsie New York 12603 (US)
Inventor: Schiable, Paul Martin
46 Hillis Terrace
Poughkeepsie New York 12603 (US)
Inventor: Standley, Charles Lamber
Frost Road Hillside Lake
Wappingers Falls New York 12590 (US)

(74) Representative: Klein, Daniel Jacques Henri
Compagnie IBM France Département de Propriété Intellectuelle
F-06610 La Gaude (FR)

EP 0 223 920 B1

Jouve, 18, rue Saint-Denis, 75001 PARIS

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the manufacture of high performance VLSI semiconductor chips in general and, more particularly, to a method for producing coplanar metal/insulator films on a substrate according to a chemical-mechanical (chem-mech) polishing technique with an improved polishing slurry. The above method may find extensive use in the fabrication of planarized multilevel metal semiconductor structures.

2. Description of the Prior Art

A semiconductor chip consists of an array of devices whose contacts are interconnected by patterns of wiring metal stripes. In VLSI chips, these metal patterns are multilayered and separated by layers of an insulating material. Interconnections between different metal wiring patterns are made by holes (or via holes), which are etched through said layers of insulating material. Typical chip designs consist of one or two wiring levels, with three wiring levels being the current state of the art. Circuit cost and performance continue to place demand on the fabrication processes in such a way that adding supplementary wiring levels can be competitive even though additional processing steps are required. However, the technique using via-holes, although widely used today, has multiple limitations and drawbacks in that, as the number of metallization layers increases wiring becomes increasingly difficult, as may be clearly understood from Fig. 1.

The semiconductor structure 10 shown in Fig. 1 is a typical example of said current state of the art technology. It is comprised of a silicon substrate 11 of a predetermined conductivity type having a patterned first insulating layer 12 of silicon dioxide ($SiO2$) thereon. The first level of metallization is represented by a metal land 13 which makes an electrical contact through via hole 14 with a region 15 of the substrate. It makes contact, for example as an ohmic contact with the emitter region of a bipolar transistor (not represented).

The second level of metallization represented by metal land 16 makes an electrical contact with metal 13 through via hole 17 of the second insulating layer 18. The structure is passivated with a third insulating layer 19. Although the structure depicted in Fig. 1 is not to scale, it gives a good idea of the very irregular surface, far from planar, which results from the standard process.

With such a structure, the known dangers are : first of a potential short at locations A between the first and second levels of metallization, due to the thinning of the insulating layer therebetween, and second the risk of a potential open circuit at locations B, due to the thinning of the metal layer at that location (so called necking effect). Those risks are unacceptable for the high standard of reliability which are required in the industry. Therefore, there is a present and serious need to improve the via-hole technique to solve the acute problem of planartzing such irregular surfaces.

A typical example of advanced planarization techniques can be found in European Patent Application No. 80302457.9 to K. Tokitomo et al assigned to Fujitsu, published under EP-A-0 023 146. According to the teachings of that particular reference, any kind of protuberances at the surface of a semiconductor structure may be removed by the following process : formation of a photoresist layer onto said surfaces, the photoresist having a substantially planar surface, and then dry etching the top surface of the structure using a reaction gas which etches both the photoresist and the material forming said protuberances at the same rate. When the material to be removed is phospho-silicate glass (PSG), the reaction gas is a mixture of a fluorine compound and oxygen, when the material is aluminum the reaction gas is a mixture of a chlorine based compound and hydrogen or oxygen. For each material, the reaction gas must be selected appropriately.

This process has several and significant disadvantages which are listed below :

1. Only the second level of metallization (and the following) are planarized, so there still remains a potential risk of necking for the second level metal land (see Fig. 5 of European Patent Application No. 80302457.9).
2. The second insulating layer is very thin at the locations where the first level metal land overlies the first insulating layer. This may cause shorts between metal lines at different levels and undesired parasitic capacitances and coupling as well (see Fig. 5 of European Patent Application No. 80302457.9).
3. The etch back operation must be controlled very accurately, because there is no natural etch stop barrier to end the process, and variations in etch rate exist within a wafer and from wafer to wafer. The

risk is to expose the top of the first level metallization (see Fig. 5 of European Patent Application No. 80302457.9).

4. Due to the absence of said etch stop barrier, the dry etching of aluminum is effected in a two step process with a change in the nature of the reaction gas (see Figs. 12-13).

More generally, plasma etching or Reactive Ion Etching (RIE) of metals with a resist planarizing medium, which appear to be the preferred methods for planarizing semiconductor devices, have limitations inherent to those techniques. First, these techniques cannot be used with all metals but only with those forming volatile reaction products. Then, as far as aluminum is concerned the process is complicated by the presence of a thin Al_2O_3 layer at the surface of the metal. It has been reported that an unpredictable initiation period is required to remove this Al_2O_3 layer, followed by a rapid, nonuniform removal of the aluminum layer itself, making this a difficult process to control. Lastly, RIE processes are complex and costly. In addition the use of a resist may also be a source of contamination.

No suggestion is known to have been made so far of using a chem-mech polishing process for planarization of metals and insulators. The use of mechanical polishing (or abrasive polishing) was recently reported in two articles authored by C. H. Scrivner, for the rapid removal of aluminum lands at the second level of metallization for testing purposes.

In the first article, published in the IBM Technical Disclosure Bulletin, Vol. 20, No. 11A, pages 4430-4431, April 1978, the special design of a test site chip is described that lends itself to easy laboratory diagnosis. To use this test site as described one must have the ability to remove the metal at the second level to isolate the via-holes. This is accomplished abrasively by parallel polishing the whole wafer. The metal is left intact in the via-holes for probing purposes. Although the composition of the polishing slurry is not disclosed, a standard polishing slurry such as a water based silica or alumina slurry could be used.

Further information concerning the use of a polishing slurry may be found in the second article published in the IBM Technical Disclosure Bulletin, Vol. 24, No. 4, Sept. 1981, page 2138. According to the latter, the test site chip or a piece of the wafer containing it is mounted on a metal stud (2.5 cm in diameter), which in turn is inserted in a commercial parallel polisher that polishes the surface of the chip. This article clearly points out the disadvantages of the previous cited technique, and in particular it mentions that the polishing step is destructive to the wafer. Also, when only a small area of the wafer is concerned, the article suggests the use of a pencil eraser dipped in a slurry of alumina powder, to manually remove the second level of metal on a limited portion of the chip.

There are a number of reasons that would have prevented one skilled in the art to apply above mechanical polishing techniques with an alumina slurry to the planarization of multilayered metal structures. First, alumina is considered to be an abrasive agent. Although used for lapping, alumina is not used for final chem-mech polishing of silicon substrates due to its higher crystal damage tendency as compared to silica slurries. Ref. D1, EP-A-013508 describes a planarization process of polysilicon isolated trenches using an alumina slurry with alkali additives to give selective chem-mech removal of the polysilicon fill relative to the Si_3N_4 etch stop layer. The polishing solution contains potassium hydroxide (KOH) and aluminum oxide (Al_2O_3) as the main constituents. The polishing step is completed when the Si_3N_4 reveals itself from said poly silicon layer which is being polished, to let the polysilicon fill only in the isolation trenches. As to Ref. D2, US-A-3911562, a similar disclosure is made. The disclosure is still directed to the polishing of polysilicon filled trenches, but a different polishing solution is used. The solution consists of ammonium fluoride (NH_4F) and copper fluoborate salts in water, and is free of alumina.

Another reason is that using mechanical polishing with a water based alumina slurry to remove an Al-Cu layer from an insulating surface does not provide a controllable process for producing metallization structures. Demonstration will be given below (see Table I) that such a slurry polishes Al-Cu and SiO_2 with equal etch rates, leading to significant removal of the insulating layer. So there is still a demand for a new and improved method of producing coplanar metal/insulator films on a substrate.

SUMMARY OF THE INVENTION

It is therefore a primary object of the invention to provide a method for producing coplanar metal/insulator films on a substrate without requiring the complex, poorly controlled, costly and contaminating dry etching planarization techniques.

It is another object of the invention to provide a method for producing coplanar metal/insulator films on a substrate according to a chem-mech technique without any limitations as to the nature of the metal or of the insulator.

It is another object of the present invention to provide a method for producing coplanar metal/insulator films on a substrate according to the chem-mech technique where fine metal geometries may be obtained.

It is still another object of the invention to provide a method for producing coplanar metal/insulator films on a substrate according to the chem-mech technique with improved selective slurries which have significantly different removal rates for the metal than for the insulator, to allow the insulator or the metal to be used as an automatic etch stop barrier in a very controllable process.

According to the present invention coplanar metal/insulator films are produced on a substrate by the method including the steps of : providing a substrate, forming on said substrate a layer of an insulating material having at least a via hole, a line recess, or a combination thereof, depositing a layer of a conductive metal onto the structure, and chem-mech polishing the top surface of the resulting structure with an acidic alumina based solution. Said layer of insulating material may be used as an automatic polishing or etch stop layer, if desired. Alternatively, a polishing stop layer per se may be used on top of the insulating material.

Where aluminum based alloys such as Al-Cu and doped or non-doped glasses such as SiO_2 are respectively used as the metal and the insulating material, the slurry is preferably comprised of an alumina powder in a diluted acid (typically HNO_3 solution) to produce a pH less than about 3. A suitable polishing stop material, if desired, is a silicon nitride film.

The above method may be used at any level of metallization in the fabrication process of multilayered metal semiconductor structures and repeated the desired number of times to produce planar structures.

Additional objects and features of the invention will become apparent from the following description in which the preferred embodiment is set forth in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a schematic cross-sectional view of a multilayered metal semiconductor structure fabricated according to standard processes and exhibiting a typical non-planar surface.

Figs. 2A and 2B illustrate the method of a first embodiment of the present invention when applied to a conductive line formed in an insulating layer to produce a coplanar metal/insulator surface.

Figs. 3A and 3B illustrate the method of the first embodiment of the present invention when applied to the formation of a metal filled via-hole formed in an insulating layer to produce a coplanar metal/insulating film.

Fig. 4 illustrates the method of the first embodiment of the present invention combining the above steps to produce a planarized multilevel metal structure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Example I

As shown in Fig. 2A, a structure 20 is represented, comprised of a substrate 21 which may be a semiconductor body or an insulating body having a substantially planar surface, with an insulating layer 22 thereon. For example, the dielectric material forming layer 22 may be sputtered silicon dioxide, the thickness of which is equal to the sum of the desired metal thickness and the underlying dielectric thickness (which can be zero). A polishing stop layer e.g. Si_3N_4 can be deposited on top of the quartz for better thickness control in polishing. Layer 22 is patterned with standard photolithographic techniques to produce the desired pattern, e.g. a trench 24. By trench is meant a recess of any arbitrary shape, which may penetrate either partially or totally the thickness of the insulating layer. The trench will be subsequentially filled with metal, to provide for instance a metal stripe 23a. A layer 23 of a high conductivity metal such as an Al-Cu alloy has been blanket deposited onto the structure and fills in particular said trench 24. The alloy is now removed down to the sputtered SiO_2 top surface leaving it intact in the trench, according to the following method.

The structure is placed in a commercially available parallel polisher such as the 18 inch diameter "Strasbaugh" single sided polisher or in the equipment described in the IBM Technical Disclosure Bulletin, Vol. 15, No. 6, November 1972, pages 1760-1761. The preferred composition of the polishing slurry may be prepared in two different ways. 1 gr. of Al_2O_3 powder (0.06 micron size) suspended in 1 liter DI water is mixed with a solution of 10 ml of HNO_3 in 90 cc of DI water, to reach a pH of about 3. Or, using two pumping systems, nitric acid is added with a needle valve to the first solution to reach the same pH. The other polishing conditions are summarized as follows :

polishing media : acidic based alumina slurry with a pH of about 3
slurry flow rate : 120 cc/min
polishing pressure : 290-1160 MPa (2-8 psi)
polishing pads : Rodel 210 I2 (from Rodel Products Corp.)

Polishing rates of the Al-Cu alloy and the sputtered SiO_2 were measured with a water based alumina slurry taken alone or in combination with different diluted acids. The results are presented in Table I below.

TABLE I

No.	Slurry Composition	Al-Cu Rate	Sputtered SiO_2 Rate	Etch Rate Ratio
1	Alumina + DI water	30 nm/min	30 nm/min	1
2	Alumina + DI water + sulfuric acid (pH 2.2)	85 nm/min	33 nm/min	3
3	Alumina + DI water + nitric acid (pH 2.2)	107 nm/min	8 nm/min	13
4	Alumina + DI water + acetic acid (pH 2.8)	150 nm/min	42.5 nm/min	3

Examination of Table I shows that addition of an acid improves either to some extent (cases 2 and 4) or significantly (case 3) the etching capabilities of a water based alumina slurry. Water based alumina slurries have been commonly used as a lapping abrasive to remove metal or prepare metal samples and apparently have been used to remove metal lands from the surface of a semiconductor structure for testing or probing purposes as explained above. However, as clear from case 1, the use of Al_2O_3 in water does not provide any removal selectivity between Al-Cu and sputtered SiO_2 as desired, meaning that the significant part of the SiO_2 layer is also removed in a poorly controllable process. In contrast, addition of an acid to produce a pH of less than about 3, and particularly the addition of HNO_3 produces a chem-mech polishing slurry which significantly increases the Al-Cu removal rate, while unexpectedly reducing simultaneously the sputtered SiO_2 removal rate, globally resulting in a large differential etch rate ratio. Although HNO_3 is a well known etchant for metals, surprisingly with the present method, the metal is not attacked in the trench at the end of the process. The above method was found reproducible in 12 separate polishing runs. In particular, a large differential etching rate ratio between Al/Cu and sputtered SiO_2 insures an excellent control over the thickness of the remaining metal in the trench, the SiO_2 layer acting as an automatic etch stop barrier.

It is clear from Fig. 2B that the top surface of metal 23A filling the trench 24 may be considered as part of a conductor line or stripe embedded in an insulating layer. The result is therefore a coplanar metal/insulator film having a very smooth surface which may find wide applications.

Example II

A limited portion of a semiconductor structure 30 is shown in Fig. 3A. It is comprised of a silicon substrate 31 of a predetermined type of conductivity passivated with a patterned insulating layer 32 of a dielectric material such as sputtered SiO_2. The insulating layer is provided with a via (or through) hole 33. By via-hole is meant a hole which penetrates totally the thickness of the insulating layer and when filled with metal provides electrical interconnection between conductive materials located at different levels. A layer 34 of a highly conductive metal such as Al-Cu has been blanket deposited on the structure. The metal makes an ohmic contact with a diffused region 35 previously formed in the silicon substrate. Although the description is made with reference to a silicon substrate, it is to be understood that the substrate might be either of the isolating type (e.g.) ceramic, glass, or a metal layer formed at a previous stage of the process.

After the chem-mech polishing technique as described with respect to Example I has been practiced the resulting structure is shown in Fig. 3B. The via hole 33 is completely filled with metal and its top surface is coplanar with the top surface of the insulating layer 32. Metal 34a may be considered for example as a stud. In this case it is therefore also produced a coplanar metal/insulator film which may be used subsequently in a multilevel interconnection scheme. Before the metal deposition, either a platinum silicide contact may be formed with region 35 or a fill metal may contact metallurgy, if desired.

Example III

Combining the steps of forming either a conductive line as taught with respect to Example I and a metal filled via hole as taught in Example II leads to the fabrication of planarized multilevel metal structures. As shown in Fig. 4, a multilevel metal structure 40 is comprised of a substrate 41 provided with a multilayered metal structure 42. The structure 42 is formed by successive application of the above described chem-mech polishing techniques, to define, conductive line 43 in insulator 44, then the metal filled via hole 45 in insulator 46 and lastly conductive line 47 in insulator 48.

Polyimide may be used as an alternative to sputtered SiO_2 as the dielectric material. The sputtered SiO_2 layer is deposited by standard sputtering techniques, the polyimide is applied by standard spin and cure processes. Since the insulating layer is applied over a substantially flat surface, the layer need not be a planarizing film, so that fast deposition techniques such as PECVD may be used where oxides are concerned. Other dielectric materials such as doped or non-doped glasses, and various polymers as well may be used. The only limitation in materials used is their compatibility with the rest of the process, and the ability to form the trench or the via-hole in the insulating layer. Both are defined by using standard photolithographic techniques. The intended metal pattern can then be transferred to the dielectric by wet or RIE etch techniques, although the latter are preferred where fine dimensions are required. Other possible techniques of forming the trench or the via-hole include projected laser assisted etching, sputtering techniques or reactive ion beam etching. It is noted that fine metal geometries may be obtained because they are defined by the dimensions of the trench or of the via-hole completed in the insulating layer. RIE of insulators is a better understood and more controllable process than RIE of metals. The present invention can take advantage of that difference. The metal can be deposited by any conformal technique, which includes sputtering, CVD or electroplating. Of course, the invention is not limited to aluminum and its alloys (Al-Si, Al-Cu) although they are preferred, other metals may be used as well. The broad concept of the invention, which is to use selective chem-mech polishing to produce coplanar metal/insulator films, being of wide application.

Chem-mech polishing processes with large removal rate ratios can be found for many combinations of metals and dielectric materials. The advantages of the chem-mech technique are that it is faster than lift-off processes, less expensive, and extendable to finer dimensions. It is applicable to a wider range of metals compared to metal RIE techniques. In contrast to dry-etch planarization techniques, chem-mech planarization produces planar structures with the upper surface of the overlying material being coplanar with the upper surface of the initially covered material, since a selective slurry will not remove significantly the latter material, which will be used as an automatic etch stop layer. It is applicable to a wider range of metals than dry-etch planarization techniques, and is more controllable.

Claims

1. A method of producing substantially coplanar metal and insulating films on a substrate (20, 30) comprising the steps of :
forming an insulating film (22, 32) of a dielectric material having a recess (24, 33) onto the top surface of said substrate ;
blanket depositing a metal film onto said insulating film to fill in particular said recess with metal ;
chem-mech polishing the top surface of the resulting structure with an acidic alumina based solution.

2. The method of claim 1 wherein the pH of said acidic solution is less than about 3.

3. The method of claim 2 wherein the acid forming said acidic solution is sulfuric acid and the pH is about 2.2.

4. The method of claim 2 wherein the acid forming said acidic solution is nitric acid and the pH is about 2. 2.

5. The method of claim 2 wherein the acid forming said acidic solution is acetic acid and the pH is about 2.8.

6. The method of any above claim wherein said metal is selected from the group including Al, Al-Si and

Al-Cu.

7. The method of any above claim wherein said dielectric material is SiO_2 or Si_3N_4.

8. The method of any above claim wherein said recess is either a via-hole or a line-shaped opening.

Ansprüche

1. Verfahren der Erzeugung wesentlich koplanarer Metallund Isolierfolien auf einem Substrat, folgende Schritte enthaltend :
Bildung eines Isolierfilms (22, 32) aus einem dielektrischen Werkstoff mit einer Vertiefung (24, 33) an der oberen fläche des besagten Substrats ;
Auftragen einer Metallfolie auf besagte Isolierfolie, um insbesondre die besagte Vertiefung mit Metall aufzufüllen ;
chemisch-mechanisches Polieren der Oberfläche der sich ergebenden Struktur mit einer Lösung auf Grundlage von Aluminiumoxid in Säure.

2. Verfahren gemäß Anspruch 1, in dem der pH der besagten Säurelösung bei weniger als 3 liegt.

3. Verfahren gemäß Anspruch 2, in dem die Säure, die die besagte saure Lösung bildet, Schwefelsäure ist und der pH ca. 2,2 beträgt.

4. Verfahren gemäß Anspruch 2, in dem die Säure, die die besagte saure Lösung bildet, Salpetersäure ist und der pH ca. 2,2 beträgt.

5. Verfahren gemäß Anspruch 2, in dem die Säure, die die besagte saure Lösung bildet, Essigsäure ist und der pH ca. 2,8 beträgt.

6. Verfahren nach einem der vorangehenden Ansprüche, in dem das besagte Metall aus der Gruppe gewählt wird, die Al, Al-Si und Al-Cu enthält.

7. Verfahren nach einem der vorangehenden Ansprüche, in dem das besagte dielektrische Material SiO_2 oder Si_3N_4 ist.

8. Verfahren gemäß einem der vorangehenden Ansprüche, in dem die besagte Öffnung entweder ein durchgehendes Loch oder ein linear ausgeführte Öffnung darstellt.

Revendications

1. Méthode de production de films métallique et isolant pratiquement co-planaires sur un substrat (20, 30), comprenant les étapes suivantes :
formation d'un film isolant (22, 32) en matériau diélectrique comportant un évidement (24, 33) sur la surface supérieure dudit substrat,
dépôt d'un film métallique sur l'ensemble dudit film isolant pour remplir, en particulier, ledit évidement de métal,
polissage mécanique et chimique de la surface supérieure de la structure résultante au moyen d'une solution acide comportant des particules d'alumine.

2. Méthode selon la revendication 1 dans laquelle le pH de ladite solution acide est inférieur à 3 environ.

3. Méthode selon la revendication 2 dans laquelle l'acide formant ladite solution acide est de l'acide sulfurique et le pH est égal à 2,2 environ.

4. Méthode selon la revendication 2 dans laquelle l'acide formant ladite solution acide est de l'acide nitrique et le pH est égal à 2,2 environ.

5. Méthode selon la revendication 2 dans laquelle l'acide formant ladite solution acide est de l'acide acétique et le pH est égal à 2,8 environ.

6. Méthode selon l'une quelconque des revendications précédentes dans laquelle ledit métal est choisi parmi le groupe comprenant l'Al, l'Al-Si et l'Al-Cu.

7. Méthode selon l'une quelconque des revendications précédentes dans laquelle ledit matériau diélectrique est du SiO_2 ou du Si_3N_4.

8. Méthode selon l'une quelconque des revendications précédentes dans laquelle ledit évidement est soit un trou d'accès, soit une ouverture en forme de tranchée.

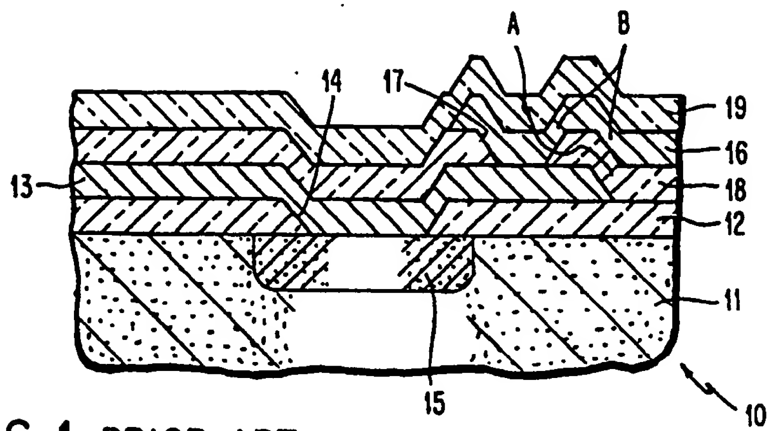

FIG. 1 PRIOR ART

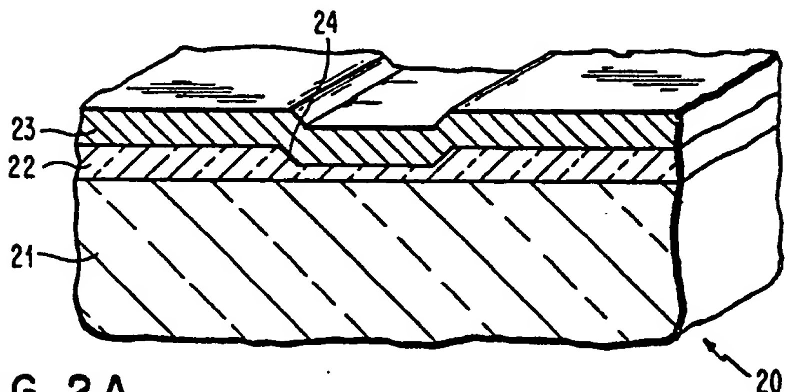

FIG. 2A

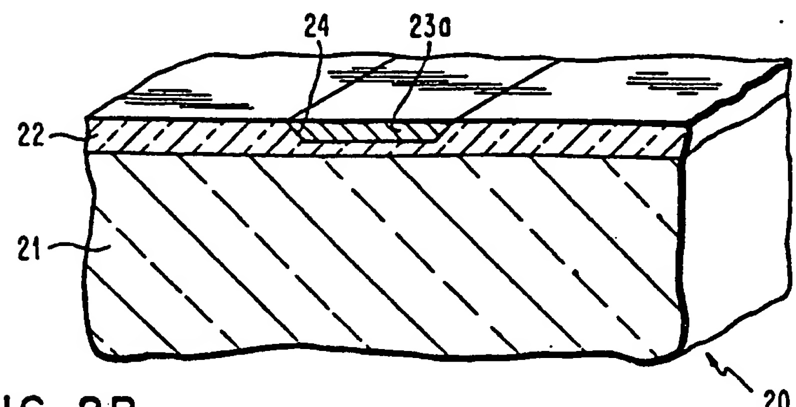

FIG. 2B

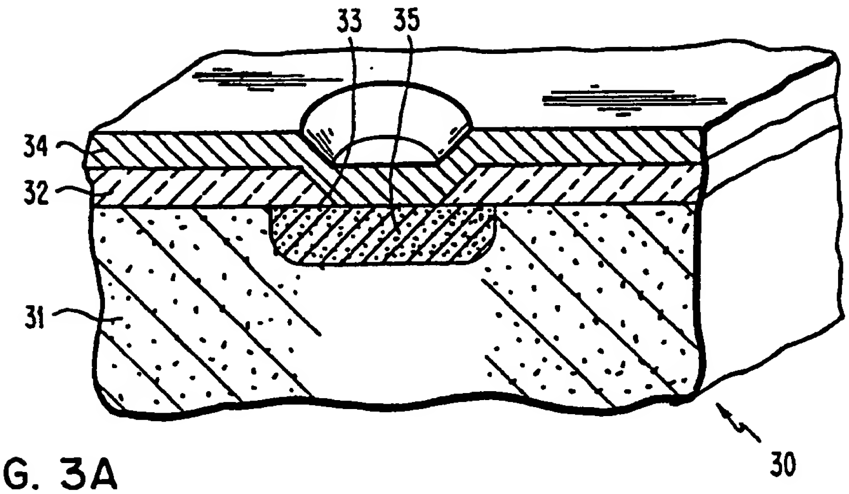

FIG. 3A

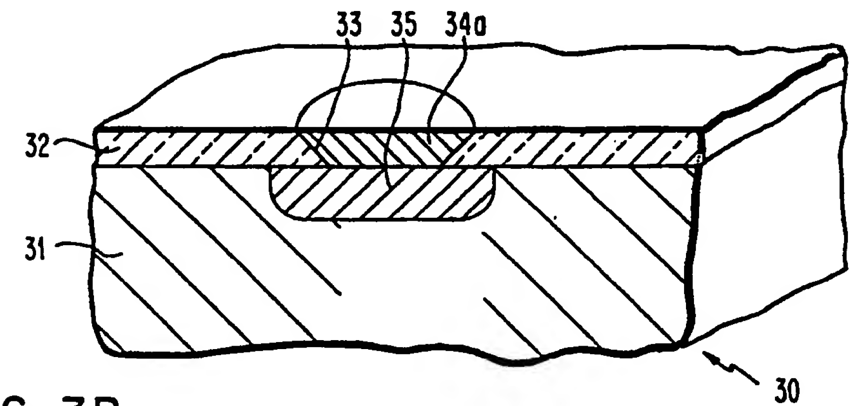

FIG. 3B

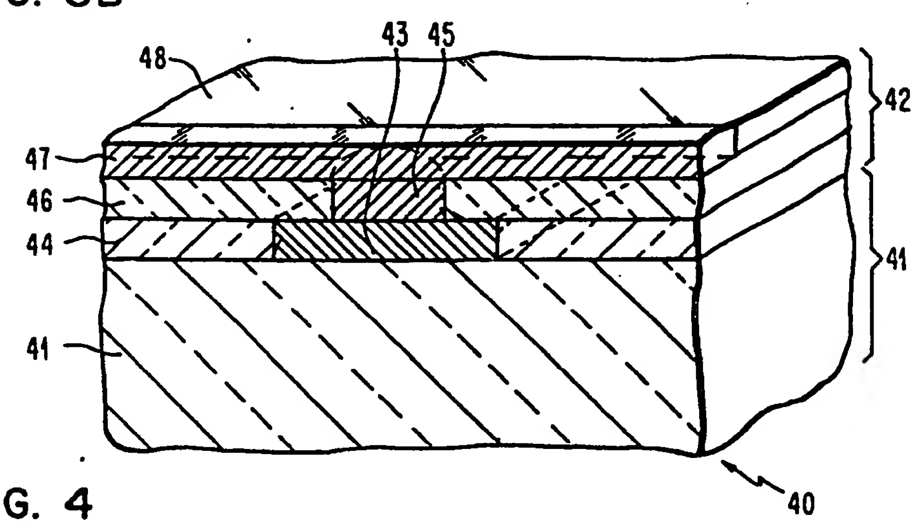

FIG. 4